AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (original) A circuit for measuring timing uncertainties in a clock signal, said circuit comprising:

a local clock buffer receiving a global clock and providing a local clock;

a delay line receiving said local clock, said local clock traversing said delay line and being provided as an output at output taps along said traversed delay line; and

a register clocked by said local clock and capturing the state of said output taps, progression of said local clock through said delay line being captured in said register.

2. (original) A circuit as in claim 1 wherein said delay line is at least 3 global clock cycles long.

3. (original) A circuit as in claim 2 wherein said delay line taps are evenly spaced along said delay line and a clock edge in said delay line is identified by a matched state at a pair of adjacent said delay line taps.

4. (canceled)

5. (currently amended) A circuit as in claim 36 [[4]] wherein said local clock is a complementary pair of local clocks, said delay line receiving a first local clock of said complementary pair of local clocks and a said remote clock is a remote said first local clock from a second said circuit as in claim 4.

6. (currently amended) A circuit as in claim 36 [[4]] wherein said delay line is a number (N) of series connected inverters, an output of said multiplexor being an input to said series connected inverters.

7. (original) A circuit as in claim 6 wherein said register is an N bit register, each bit receiving an output of one of said series connected inverters.

8. (original) A circuit as in claim 6 wherein one of said series connected inverters is an adjustable delay inverter selectably varying delay in said delay line.

9. (currently amended) A circuit as in claim 36 [[4]] wherein said register is an N bit register, said circuit further comprising:

a second register, said second register being an N-1 bit register selectively receiving the contents of said N bit register.

10. (original) A circuit as in claim 9, said circuit further comprising:

a compare receiving the contents of said second register and detecting clock edges falling outside of an acceptable range.

11. (original) A circuit as in claim 10 wherein said compare

compares second register bit patterns against a selectable signature bit pattern indicating expected edge locations, and

generates an interrupt signal for a service processor if a clock edge is determined to occur other than in an expected edge location.

12. (original) A circuit as in claim 9 further comprising:

an adjustable delay receiving an output from said multiplexor and selectably delaying said output, said selectably delayed output being a time shifted one of said local clock and said remote clock.

13. (original) A circuit as in claim 9 wherein contents of said second register may be held over a selected number of clock cycles.

14. (original) A circuit as in claim 9 wherein contents of said second register may be shifted out in a functional shift without stopping the clocks or using a scan path.

15. (original) A circuit as in claim 9 wherein clock edges may be accumulated over a selected number of clock cycles.

16. (original) A circuit as in claim 15 wherein accumulated said clock edges indicate a clock jitter range.

17. (original) A circuit as in claim 16 wherein accumulated said clock edges indicate clock skew and power supply noise related timing uncertainty in each cycle.

18. (currently amended) A circuit as in claim 36 [[4]] measuring jitter, skew and power supply noise related timing uncertainty in each cycle.

19. (currently amended) A circuit as in claim 36 [[4]] further comprising a start counter delaying data logging until after a selected number of clock cycles.

20. (original) A circuit for measuring timing uncertainties in a clocked data path, said circuit comprising a cross coupled pair of timing variation measurement circuits, each of said cross coupled pair comprising:

a local clock buffer receiving a global clock and providing a complementary pair of local clocks;

a multiplexor receiving a first local clock of said complementary pair of local clocks and a remote clock, said remote clock being said first local clock from another of

said cross coupled pair, said multiplexor selectively providing said first local clock and said remote clock as a multiplexor output;

a delay line receiving a timing signal from said multiplexor output, said timing signal traversing said delay line and being provided as an output at output taps along said traversed delay line; and

a capture register clocked by said complementary pair, connected to said output taps and receiving said output from said output taps, progression of said timing being captured in said capture register.

21. (original) A circuit as in claim 20 wherein each said delay line is at least 3 clock cycles long.

22. (original) A circuit as in claim 21 wherein said delay line taps are evenly spaced along said each delay line and a timing signal edge in said delay line is identified by a matched pair of adjacent said delay line taps.

23. (original) A circuit as in claim 21wherein each said delay line is a number (N) of series connected inverters, an output of said multiplexor being provided to said series connected inverters.

24. (original) A circuit as in claim 23 wherein each said capture register is an N bit register, an input to each bit of said each capture register is connected to an output of one of said series connected inverters.

25. (original) A circuit as in claim 24 wherein one of said series connected inverters is an adjustable delay inverter selectably varying delay in said delay line.

26. (original) A circuit as in claim 24, each of said cross coupled pair further comprising:

a second register, said second register being an N-1 bit register selectively receiving the contents of said N bit register; and

a compare receiving the contents of said second register and detecting clock edges falling outside of an acceptable range.

27. (original) A circuit as in claim 26 wherein said compare

compares capture register bit patterns against a selectable signature bit pattern indicating expected edge locations, and

generates an interrupt signal to a service processor if a clock edge is determined to occur other than in an expected edge location.

28. (original) A circuit as in claim 26, each of said cross coupled pair further comprising:

data logging control logic receiving a hold control signal selectively holding contents of said second register over a selected number of clock cycles and a sticky input accumulating clock edges in said second register over a selected number of clock cycles.

29. (original) A circuit as in claim 28 measuring jitter, skew and power supply noise related timing uncertainty in each cycle.

30. (original) A circuit as in claim 25 further comprising a start counter delaying data logging until after a selected number of clock cycles.

31 – 35 (canceled)

36. (new) A circuit for measuring timing uncertainties in a clock signal, said circuit comprising:

a local clock buffer receiving a global clock and providing a local clock;

a multiplexor receiving said local clock and a remote clock, said multiplexor selectively providing said local clock and said remote clock;

a delay line receiving said local clock and said remote clock from said multiplexor, said local clock traversing said delay line and being provided as an output at output taps along said traversed delay line; and

a register clocked by said local clock and capturing the state of said output taps, progression of said local clock through said delay line being captured in said register.

37. (new) A circuit as in claim 36 wherein said delay line is at least 3 global clock cycles long.

38. (new) A circuit as in claim 37 wherein said delay line taps are evenly spaced along said delay line and a clock edge in said delay line is identified by a matched state at a pair of adjacent said delay line taps.